Si8640/41/42/45

LOW-POWER QUAD-CHANNEL DIGITAL ISOLATOR

Features

- High-speed operation
  - DC to 150 Mbps
- No start-up initialization required
- Wide Operating Supply Voltage
  - 2.5–5.5 V
- Up to 5000 V_{RMS} isolation
- 60-year life at rated working voltage
- High electromagnetic immunity
- Ultra low power (typical)
  5 V Operation
  - 1.6 mA per channel at 1 Mbps
  - 5.5 mA per channel at 100 Mbps
  2.5 V Operation
  - 1.5 mA per channel at 1 Mbps
  - 3.5 mA per channel at 100 Mbps
- Tri-state outputs with ENABLE
- Schmitt trigger inputs
- Selectable fail-safe mode
  - Default high or low output (ordering option)
- Precise timing (typical)
  - 10 ns propagation delay
  - 1.5 ns pulse width distortion
  - 0.5 ns channel-channel skew
  - 2 ns propagation delay skew
  - 5 ns minimum pulse width
- Transient Immunity 50 kV/µs
- AEC-Q100 qualification
- Wide temperature range
  - –40 to 125 °C
- RoHS-compliant packages
  - SOIC-16 wide body
  - SOIC-16 narrow body
  - QSOP-16

Ordering Information:
See page 26.

Applications

- Industrial automation systems
- Medical electronics
- Hybrid electric vehicles
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communications systems

Safety Regulatory Approvals

- UL 1577 recognized
  - Up to 5000 V_{RMS} for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)
  - EN60950-1 (reinforced insulation)

Description

Silicon Lab's family of ultra-low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages over legacy isolation technologies. The operating parameters of these products remain stable across wide temperature ranges and throughout device service life for ease of design and highly uniform performance. All device versions have Schmitt trigger inputs for high noise immunity and only require VDD bypass capacitors.

Data rates up to 150 Mbps are supported, and all devices achieve propagation delays of less than 10 ns. Enable inputs provide a single point control for enabling and disabling output drive. Ordering options include a choice of isolation ratings (3.75 and 5 kV) and a selectable fail-safe operating mode to control the default output state during power loss. All products >1 kV_{RMS} are safety certified by UL, CSA, and VDE, and products in wide-body packages support reinforced insulation withstanding up to 5 kV_{RMS}.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	150 Mbps, 15 pF, 5 V	–40	25	125	ºC
Supply Voltage	V_{DD1}		2.5	—	5.5	V
	V_{DD2}		2.5	—	5.5	V

***Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 2. Electrical Characteristics

(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Negative-Going Lockout Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	—	2.0	—	µA

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics (Continued)
(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Current (All inputs 0 V or at Supply)						
Si8640Bx, Ex, Si8645Bx						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.0	1.6	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.4	3.8	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	6.1	9.2	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	2.5	4.0	
Si8641Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.4	2.2	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.3	3.7	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	5.2	7.8	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	3.6	5.4	
Si8642Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.8	2.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	1.8	2.9	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	4.4	6.6	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.4	6.6	
1 Mbps Supply Current (All inputs = 500 kHz square wave, CI = 15 pF on all outputs)						
Si8640Bx, Ex, Si8645Bx						
V_{DD1}			—	3.6	5.0	mA
V_{DD2}			—	2.9	4.0	
Si8641Bx, Ex						
V_{DD1}			—	3.4	4.8	mA
V_{DD2}			—	3.3	4.6	
Si8642Bx, Ex						
V_{DD1}			—	3.3	4.6	mA
V_{DD2}			—	3.3	4.6	
10 Mbps Supply Current (All inputs = 5 MHz square wave, CI = 15 pF on all outputs)						
Si8640Bx, Ex, Si8645Bx						
V_{DD1}			—	3.6	5.0	mA
V_{DD2}			—	4.0	5.6	
Si8641Bx, Ex						
V_{DD1}			—	3.7	5.2	mA
V_{DD2}			—	4.1	5.8	
Si8642Bx, Ex						
V_{DD1}			—	3.9	5.4	mA
V_{DD2}			—	3.9	5.4	

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics (Continued)
(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8640Bx, Ex, Si8645Bx V_{DD1} V_{DD2}			 — —	 3.6 17.5	 5.0 22.8	mA
Si8641Bx, Ex V_{DD1} V_{DD2}			 — —	 7.3 14.3	 9.8 18.5	mA
Si8642Bx, Ex V_{DD1} V_{DD2}			 — —	 11 11	 14.3 14.3	mA
Timing Characteristics						
Si864xBx, Ex						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	5.0	8.0	13	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	0.2	4.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 7	—	350	—	ps
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	35	50	—	kV/µs
Enable to Data Valid	t_{en1}	See Figure 1	—	6.0	11	ns
Enable to Data Tri-State	t_{en2}	See Figure 1	—	8.0	12	ns
Startup Time[3]	t_{SU}		—	15	40	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

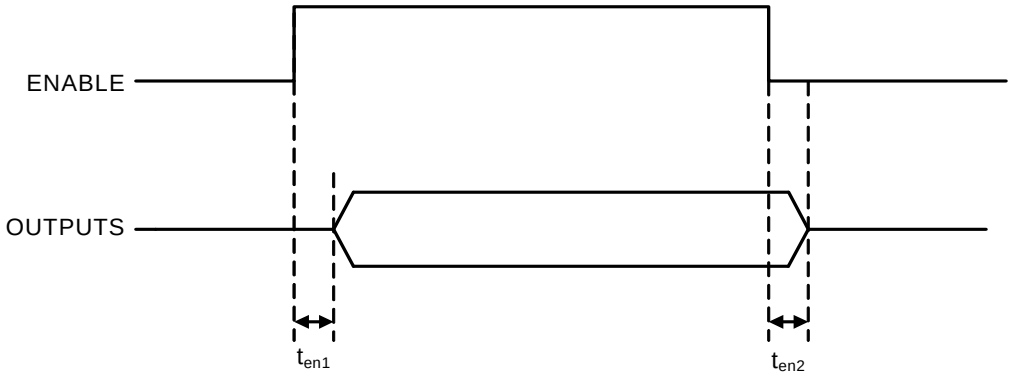


Figure 1. ENABLE Timing Diagram

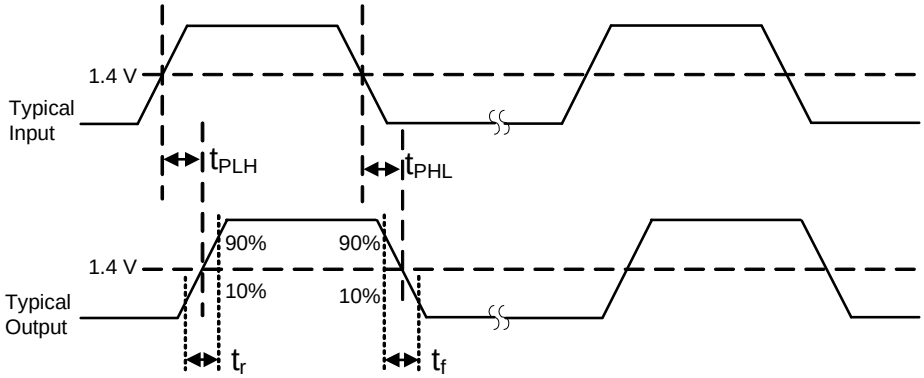


Figure 2. Propagation Delay Timing

Table 3. Electrical Characteristics

(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Negative-Going Lockout Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8640Bx, Ex, Si8645Bx						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.0	1.6	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.4	3.8	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	6.1	9.2	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	2.5	4.0	
Si8641Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.4	2.2	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.3	3.7	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	5.2	7.8	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	3.6	5.4	
Si8642Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.8	2.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	1.8	2.9	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	4.4	6.6	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.4	6.6	

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1 Mbps Supply Current (All inputs = 500 kHz square wave, CI = 15 pF on all outputs)						
Si8640Bx, Ex, Si8645Bx						
V_{DD1}			—	3.6	5.0	mA
V_{DD2}			—	2.9	4.0	
Si8641Bx, Ex						
V_{DD1}			—	3.4	4.8	mA
V_{DD2}			—	3.3	4.6	
Si8642Bx, Ex						
V_{DD1}			—	3.3	4.6	mA
V_{DD2}			—	3.3	4.6	
10 Mbps Supply Current (All inputs = 5 MHz square wave, CI = 15 pF on all outputs)						
Si8640Bx, Ex, Si8645Bx						
V_{DD1}			—	3.6	5.0	mA
V_{DD2}			—	3.4	4.7	
Si8641Bx, Ex						
V_{DD1}			—	3.5	4.9	mA
V_{DD2}			—	3.6	5.1	
Si8642Bx, Ex						
V_{DD1}			—	3.6	5.0	mA
V_{DD2}			—	3.6	5.0	
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8640Bx, Ex, Si8645Bx						
V_{DD1}			—	3.6	5.0	mA
V_{DD2}			—	12.3	15.9	
Si8641Bx, Ex						
V_{DD1}			—	5.9	7.9	mA
V_{DD2}			—	10.3	13.4	
Si8642Bx, Ex						
V_{DD1}			—	8.2	10.7	mA
V_{DD2}			—	8.2	10.7	

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
Si864xBx, Ex						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	5.0	8.0	13	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	0.2	4.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Peak eye diagram jitter	$t_{JIT(PK)}$	See Figure 7	—	350	—	ps
Common Mode Transient Immunity at Logic Low Output	CMTI	$V_I = V_{DD}$ or 0 V	35	50	—	kV/µs
Enable to Data Valid	t_{en1}	See Figure 1	—	6.0	11	ns
Enable to Data Tri-State	t_{en2}	See Figure 1	—	8.0	12	ns
Startup Time[3]	t_{SU}		—	15	40	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics

(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Negative-Going Lockout Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	loh = –4 mA	V_{DD1}, V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	lol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8640Bx, Ex, Si8645Bx						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.0	1.6	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.4	3.8	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	6.1	9.2	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	2.5	4.0	
Si8641Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.4	2.2	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.3	3.7	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	5.2	7.8	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	3.6	5.4	
Si8642Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.8	2.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	1.8	2.9	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	4.4	6.6	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.4	6.6	

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1 Mbps Supply Current (All inputs = 500 kHz square wave, CI = 15 pF on all outputs)						
Si8640Bx, Ex, Si8645Bx						
V_{DD1}			—	3.6	5.0	mA
V_{DD2}			—	2.9	4.0	
Si8641Bx, Ex						
V_{DD1}			—	3.4	4.8	mA
V_{DD2}			—	3.3	4.6	
Si8642Bx, Ex						
V_{DD1}			—	3.3	4.6	mA
V_{DD2}			—	3.3	4.6	
10 Mbps Supply Current (All inputs = 5 MHz square wave, CI = 15 pF on all outputs)						
Si8640Bx, Si8645Bx						
V_{DD1}			—	3.6	5.0	mA
V_{DD2}			—	3.1	4.3	
Si8641Bx, Ex						
V_{DD1}			—	3.5	4.8	mA
V_{DD2}			—	3.4	4.8	
Si8642Bx, Ex						
V_{DD1}			—	3.4	4.8	mA
V_{DD2}			—	3.4	4.8	
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8640Bx, Ex, Si8645Bx						
V_{DD1}			—	3.6	5.0	mA
V_{DD2}			—	9.9	12.8	
Si8641Bx, Ex						
V_{DD1}			—	5.2	7.0	mA
V_{DD2}			—	8.5	11.1	
Si8642Bx, Ex						
V_{DD1}			—	6.9	9.0	mA
V_{DD2}			—	6.9	9.0	

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
Si864xBx, Ex						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	5.0	8.0	14	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	0.2	5.0	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	5.0	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 7	—	350	—	ps
Common Mode Transient Immunity at Logic Low Output	CMTI	$V_I = V_{DD}$ or 0 V	35	50	—	kV/µs
Enable to Data Valid	t_{en1}	See Figure 1	—	6.0	11	ns
Enable to Data Tri-State	t_{en2}	See Figure 1	—	8.0	12	ns
Startup Time[3]	t_{SU}		—	15	40	µs

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Regulatory Information*

CSA
The Si864x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 125 V_{RMS} reinforced insulation working voltage; up to 380 V_{RMS} basic insulation working voltage.
VDE
The Si864x is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 1200 V_{peak} for basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si864x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
***Note:** Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1 sec. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec. For more information, see "5. Ordering Guide" on page 26.

Table 6. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Nominal Air Gap (Clearance)[1]	L(IO1)		8.0	4.9	3.6	mm
Nominal External Tracking (Creepage)[1]	L(IO2)		8.0	4.01	3.6	mm
Minimum Internal Gap (Internal Clearance)			0.014	0.011	0.008	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	600	V_{RMS}
Erosion Depth	ED		0.019	0.019	0.031	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	2.0	2.0	2.0	pF
Input Capacitance[3]	C_I		4.0	4.0	4.0	pF

Notes:
1. The values in this table correspond to the nominal creepage and clearance values. VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 and QSOP-16 packages and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component-level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-16, 3.6 mm for QSOP-16 packages and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si86xx is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 7. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Conditions	Specification	
		NB SOIC-16	WB SOIC-16
Basic Isolation Group	Material Group	I	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III	I-IV
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II	I-III
	Rated Mains Voltages ≤ 600 V_{RMS}	I-II	I-III

Table 8. IEC 60747-5-2 Insulation Characteristics for Si86xxxx*

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB SOIC-16	NB SOIC-16	
Maximum Working Insulation Voltage	V_{IORM}		1200	630	Vpeak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	2250	1182	
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	6000	Vpeak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The Si86xxxx provides a climate classification of 40/125/21.

Table 9. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Min	Typ	Max		Unit
					WB SOIC-16	NB SOIC-16	
Case Temperature	T_S		—	—	150	150	°C
Safety Input, Output, or Supply Current	I_S	θ_{JA} = 100 °C/W (WB SOIC-16), 105 °C/W (NB SOIC-16, QSOP-16), V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	—	—	220	210	mA
Device Power Dissipation[2]	P_D		—	—	275	275	mW

Notes:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 3 and 4.
2. The Si86xx is tested with VDD1 = VDD2 = 5.5 V, TJ = 150 ºC, CL = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 10. Thermal Characteristics

Parameter	Symbol	Test Condition	WB SOIC-16	NB SOIC-16 QSOP-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}		100	105	ºC/W

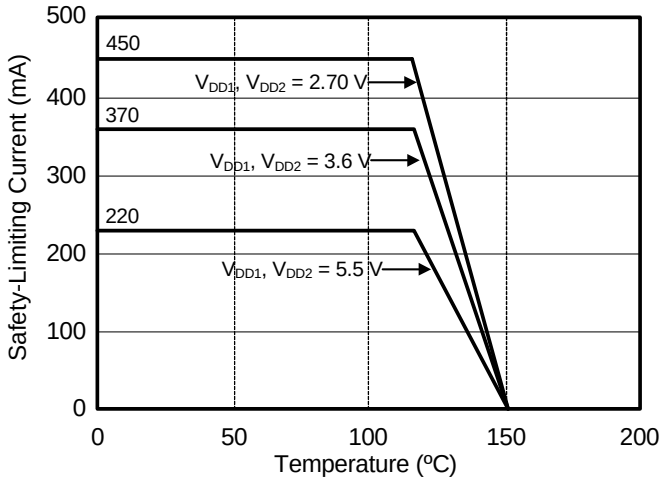


Figure 3. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

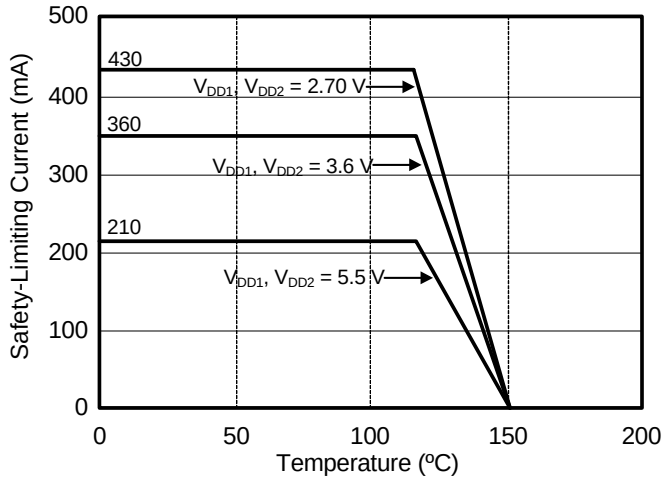


Figure 4. (NB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

Table 11. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	150	ºC
Ambient Temperature Under Bias	T_A	–40	—	125	ºC
Junction Temperature	T_J	—	—	150	°C
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	—	7.0	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	I_O	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	ºC
Maximum Isolation (Input to Output) (1 sec) NB SOIC-16, QSOP-16		—	—	4500	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) WB SOIC-16		—	—	6500	V_{RMS}

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may degrade performance.
2. VDE certifies storage temperature from –40 to 150 °C.

2. Functional Description

2.1. Theory of Operation

The operation of an Si864x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si864x channel is shown in Figure 5.

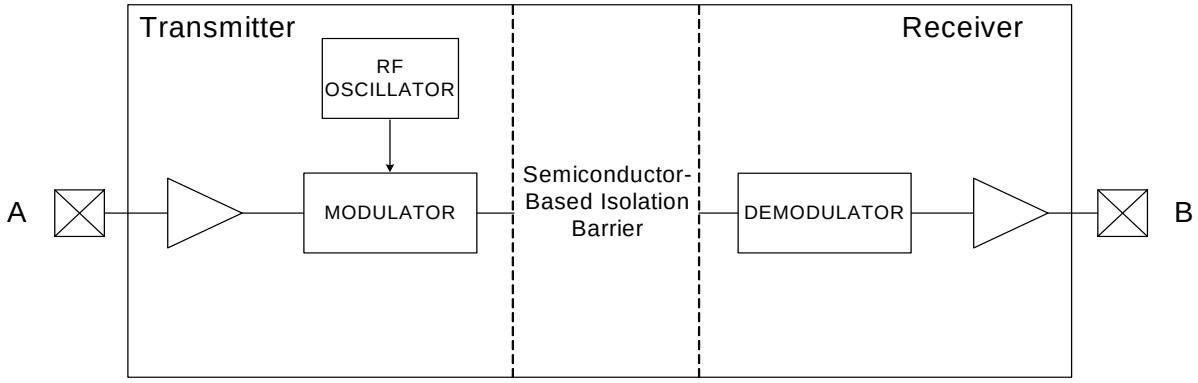


Figure 5. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 6 for more details.

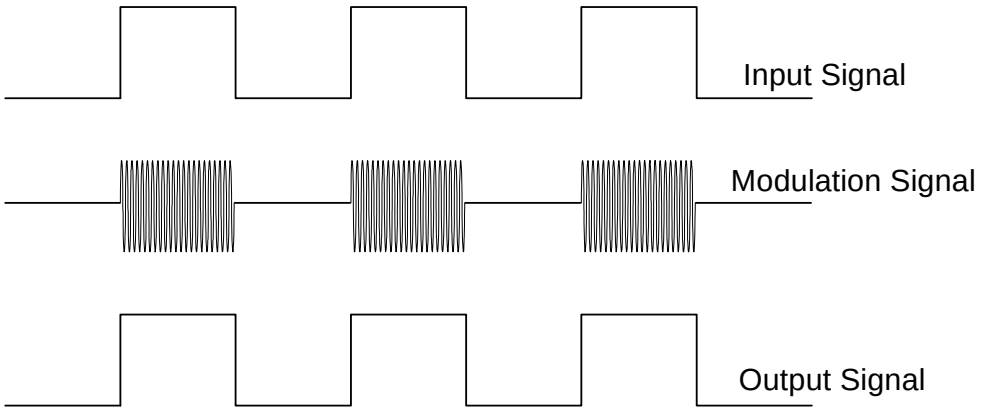


Figure 6. Modulation Scheme

2.2. Eye Diagram

Figure 7 illustrates an eye-diagram taken on an Si8640. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8640 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 350 ps peak jitter were exhibited.

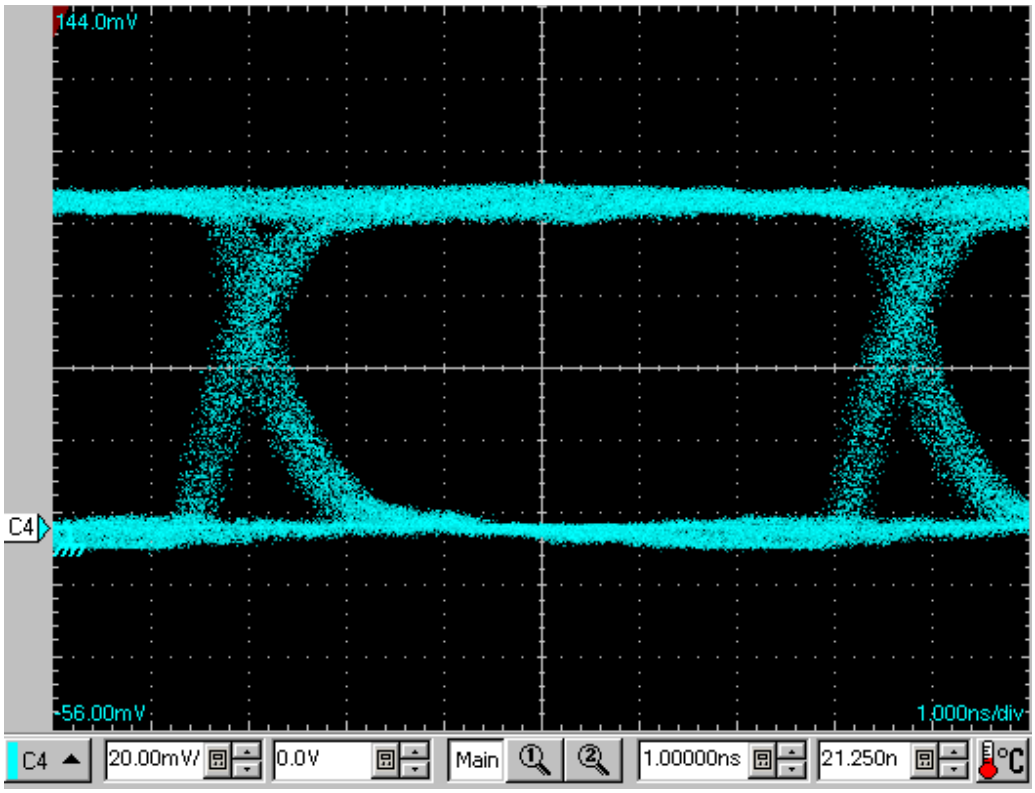


Figure 7. Eye Diagram

3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 8, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Refer to Table 12 to determine outputs when power supply (VDD) is not present. Additionally, refer to Table 13 for logic conditions when enable pins are used.

Table 12. Si86xx Logic Operation

V_I Input[1,2]	EN Input[1,2,3,4]	VDDI State[1,5,6]	VDDO State[1,5,6]	V_O Output[1,2]	Comments
H	H or NC	P	P	H	Enabled, normal operation.
L	H or NC	P	P	L	
X[7]	L	P	P	Hi-Z[8]	Disabled.
X[7]	H or NC	UP	P	L[9] H[9]	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X[7]	L	UP	P	Hi-Z[8]	Disabled.
X[7]	X[7]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs, if EN is in either the H or NC state. Upon transition of VDDO from unpowered to powered, V_O returns to Hi-Z within 1 µs if EN is L.

Notes:

1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals. EN is the enable control input located on the same output side.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. It is recommended that the enable inputs be connected to an external logic high or low level when the Si86xx is operating in noisy environments.
4. No Connect (NC) replaces EN1 on Si8640/45. No Connect replaces EN2 on the Si8645. No Connects are not internally connected and can be left floating, tied to VDD, or tied to GND.
5. “Powered” state (P) is defined as 2.5 V < VDD < 5.5 V.
6. “Unpowered” state (UP) is defined as VDD = 0 V.
7. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
8. When using the enable pin (EN) function, the output pin state is driven into a high-impedance state when the EN pin is disabled (EN = 0).
9. See "5. Ordering Guide" on page 26 for details. This is the selectable fail-safe operating mode (ordering option). Some devices have default output state = H, and some have default output state = L, depending on the ordering part number (OPN). For default high devices, the data channels have pull-ups on inputs/outputs. For default low devices, the data channels have pull-downs on inputs/outputs.

Table 13. Enable Input Truth[1]

P/N	EN1[1,2]	EN2[1,2]	Operation
Si8640	—	H	Outputs B1, B2, B3, B4 are enabled and follow the input state.
	—	L	Outputs B1, B2, B3, B4 are disabled and in high impedance state.[3]
Si8641	H	X	Output A4 enabled and follows the input state.
	L	X	Output A4 disabled and in high impedance state.[3]
	X	H	Outputs B1, B2, B3 are enabled and follow the input state.
	X	L	Outputs B1, B2, B3 are disabled and in high impedance state.[3]
Si8642	H	X	Outputs A3 and A4 are enabled and follow the input state.
	L	X	Outputs A3 and A4 are disabled and in high impedance state.[3]
	X	H	Outputs B1 and B2 are enabled and follow the input state.
	X	L	Outputs B1 and B2 are disabled and in high impedance state.[3]
Si8645	—	—	Outputs B1, B2, B3, B4 are enabled and follow the input state.

Notes:

1. Enable inputs EN1 and EN2 can be used for multiplexing, for clock sync, or other output control. EN1, EN2 logic operation is summarized for each isolator product in Table 13. These inputs are internally pulled-up to local VDD by a 2 µA current source allowing them to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do not connect circuit traces to EN1 or EN2 if they are left floating. If EN1, EN2 are unused, it is recommended they be connected to an external logic level, especially if the Si86xx is operating in a noisy environment.
2. X = not applicable; H = Logic High; L = Logic Low.
3. When using the enable pin (EN) function, the output pin state is driven into a high-impedance state when the EN pin is disabled (EN = 0).

3.1. Device Startup

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs.

3.2. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when V_{DD1} falls below $V_{DD1(UVLO–)}$ and exits UVLO when V_{DD1} rises above $V_{DD1(UVLO+)}$. Side B operates the same as Side A with respect to its V_{DD2} supply.

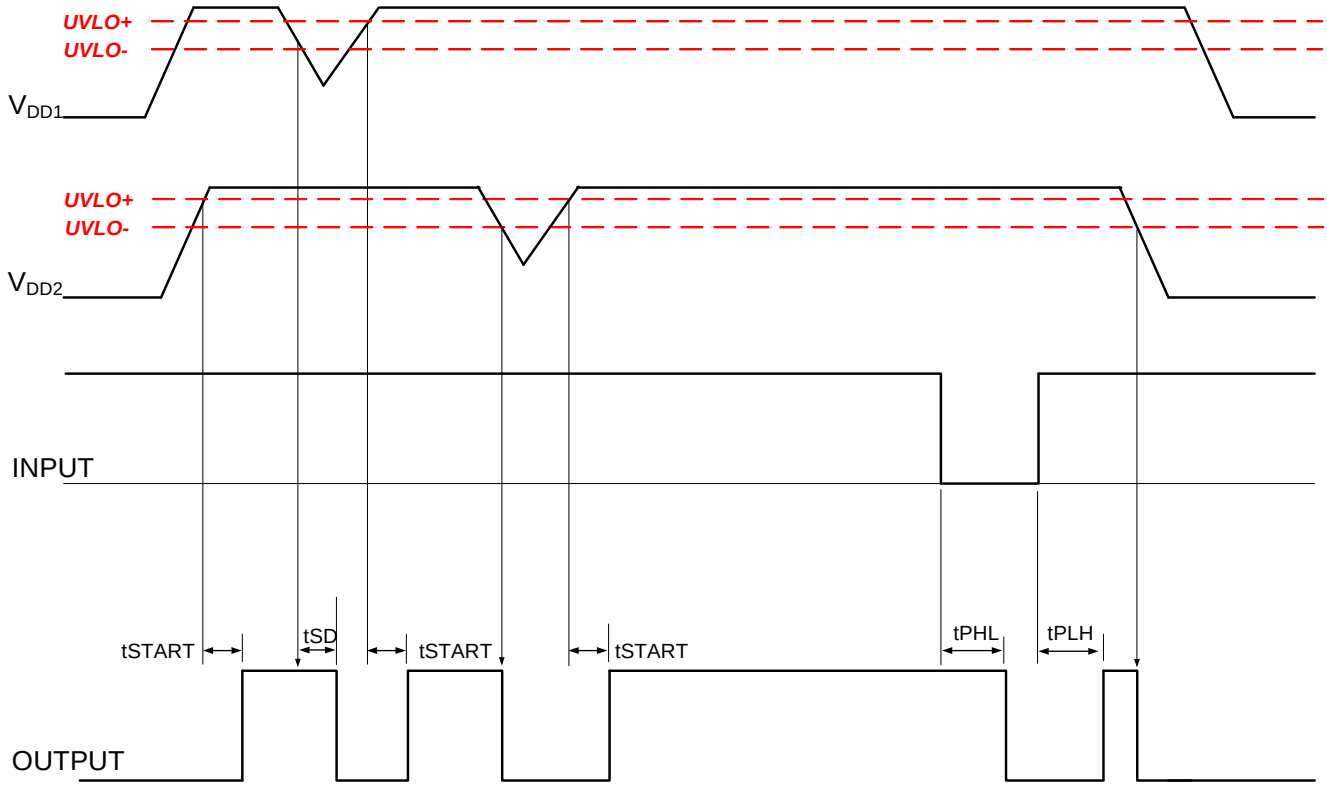


Figure 8. Device Behavior during Normal Operation

3.3. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 5 on page 14 and Table 6 on page 14 detail the working voltage and creepage/clearance capabilities of the Si86xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.3.1. Supply Bypass

The Si864x family requires a 0.1 µF bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

3.3.2. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

3.4. Fail-Safe Operating Mode

Si86xx devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is unpowered) can either be a logic high or logic low when the output supply is powered. See Table 12 on page 20 and "5. Ordering Guide" on page 26 for more information.

3.5. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Tables 2, 3, and 4 for actual specification limits.

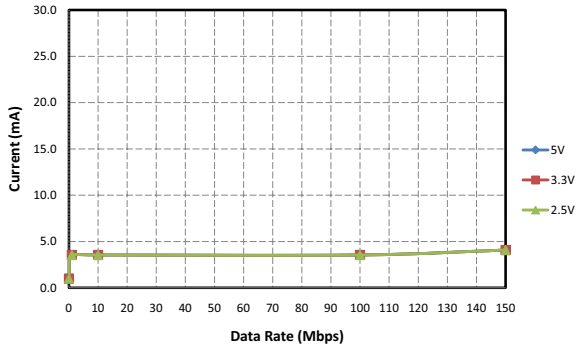


Figure 9. Si8640/45 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation

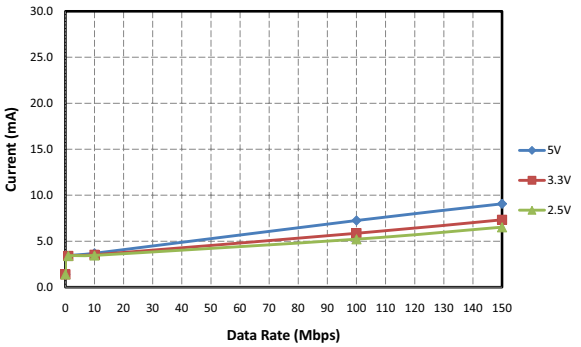


Figure 10. Si8641 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation

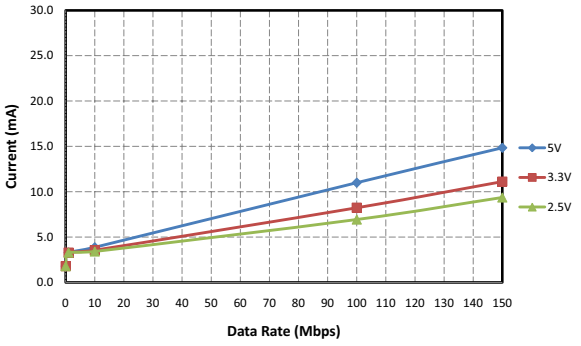


Figure 11. Si8642 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

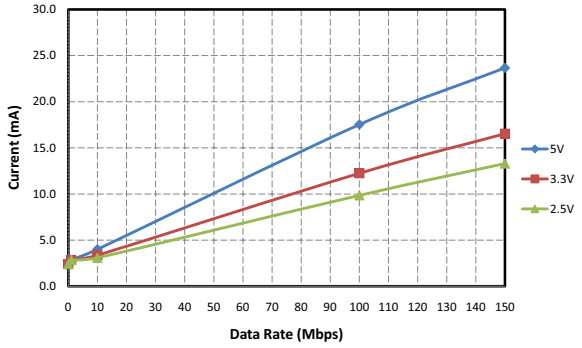


Figure 12. Si8640/45 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V

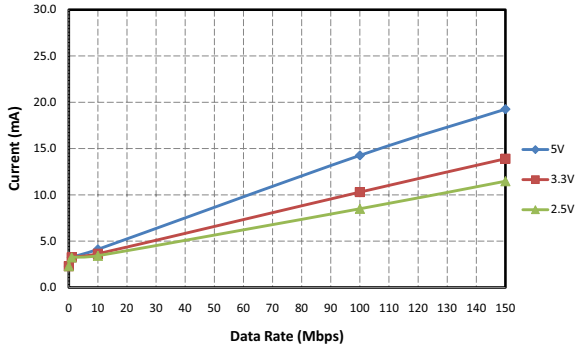


Figure 13. Si8641 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

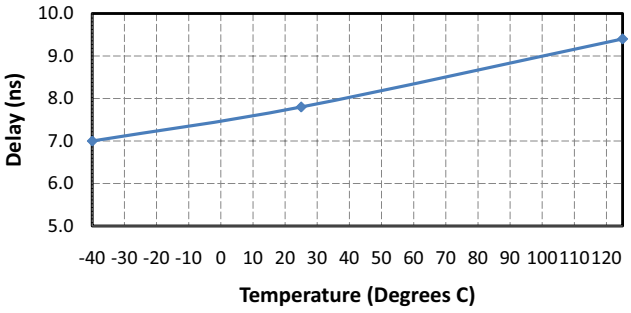
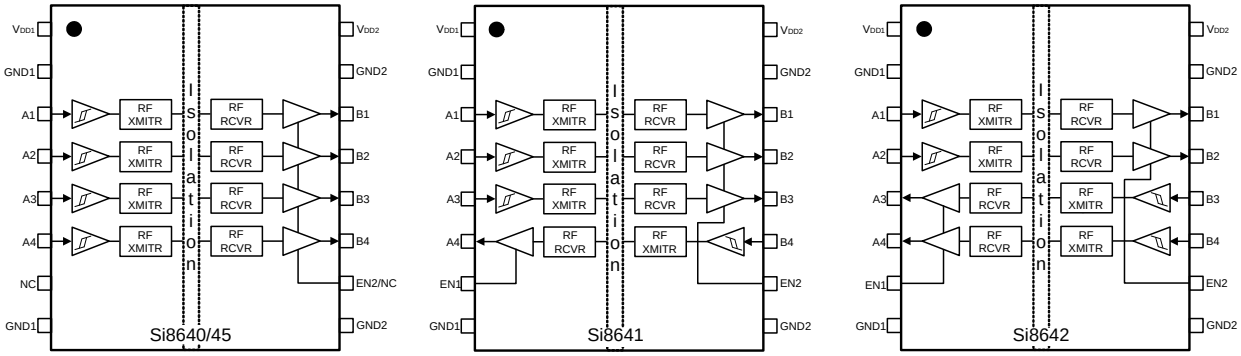


Figure 14. Propagation Delay vs. Temperature

4. Pin Descriptions



Name	SOIC-16 Pin#	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
GND1	2[1]	Ground	Side 1 ground.
A1	3	Digital Input	Side 1 digital input.
A2	4	Digital Input	Side 1 digital input.
A3	5	Digital I/O	Side 1 digital input or output.
A4	6	Digital I/O	Side 1 digital input or output.
EN1/NC[2]	7	Digital Input	Side 1 active high enable. NC on Si8640/45.
GND1	8[1]	Ground	Side 1 ground.
GND2	9[1]	Ground	Side 2 ground.
EN2/NC[2]	10	Digital Input	Side 2 active high enable. NC on Si8645.
B4	11	Digital I/O	Side 2 digital input or output.
B3	12	Digital I/O	Side 2 digital input or output.
B2	13	Digital Output	Side 2 digital output.
B1	14	Digital Output	Side 2 digital output.
GND2	15[1]	Ground	Side 2 ground.
V_{DD2}	16	Supply	Side 2 power supply.

Notes:

1. For narrow-body devices, Pin 2 and Pin 8 GND must be externally connected to respective ground. Pin 9 and Pin 15 must also be connected to external ground.
2. No Connect. These pins are not internally connected. They can be left floating, tied to V_{DD} or tied to GND.

5. Ordering Guide

Table 14. Ordering Guide for Valid OPNs[1,2]

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Max Data Rate (Mbps)	Default Output State	Isolation rating (kV)	Temp (°C)	Package
Si8640BC-B-IS1	4	0	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8640BD-B-IS	4	0	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8640EC-B-IS1	4	0	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8640ED-B-IS	4	0	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8641BA-B-IU	3	1	150	Low	1.0	–40 to 125 °C	QSOP-16
Si8641BA-C-IU	3	1	150	Low	1.0	–40 to 125 °C	QSOP-16
Si8641BC-B-IS1	3	1	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8641BD-B-IS	3	1	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8641EC-B-IS1	3	1	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8641ED-B-IS	3	1	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8642BA-B-IU	2	2	150	Low	1.0	–40 to 125 °C	QSOP-16
Si8642BA-C-IU	2	2	150	Low	1.0	–40 to 125 °C	QSOP-16
Si8642BC-B-IS1	2	2	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8642BD-B-IS	2	2	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8642EC-B-IS1	2	2	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8642ED-B-IS	2	2	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8645BA-B-IU	4	0	150	Low	1.0	–40 to 125 °C	QSOP-16
Si8645BA-C-IU	4	0	150	Low	1.0	–40 to 125 °C	QSOP-16
Si8645BC-B-IS1	4	0	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8645BD-B-IS	4	0	150	Low	5.0	–40 to 125 °C	WB SOIC-16

Notes:

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
   Moisture sensitivity level is MSL3 for wide-body SOIC-16 packages.
   Moisture sensitivity level is MSL2A for narrow-body SOIC-16 packages.
   Moisture sensitivity level is MSL2A for QSOP-16 packages.
2. All devices >1 kV_{RMS} are AEC-Q100 qualified.

6. Package Outline: 16-Pin Wide Body SOIC

Figure 15 illustrates the package details for the Si864x Digital Isolator. Table 15 lists the values for the dimensions shown in the illustration.

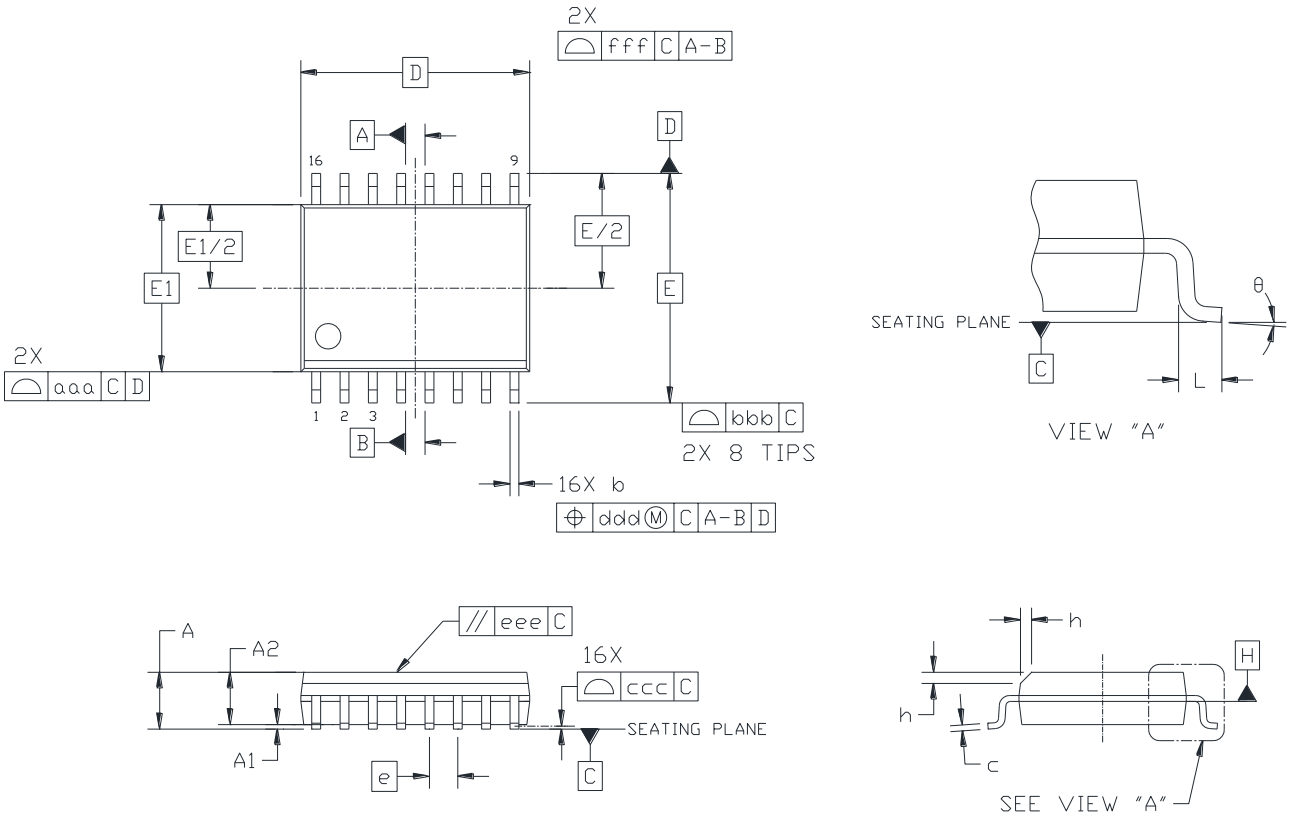


Figure 15. 16-Pin Wide Body SOIC

Table 15. Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

7. Land Pattern: 16-Pin Wide-Body SOIC

Figure 16 illustrates the recommended land pattern details for the Si864x in a 16-pin wide-body SOIC. Table 16 lists the values for the dimensions shown in the illustration.

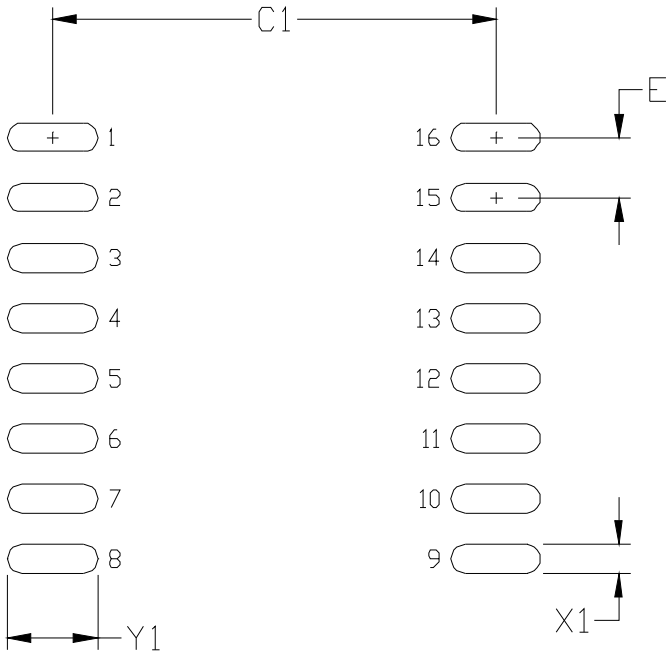


Figure 16. 16-Pin SOIC Land Pattern

Table 16. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8. Package Outline: 16-Pin Narrow Body SOIC

Figure 17 illustrates the package details for the Si864x in a 16-pin narrow-body SOIC (SO-16). Table 17 lists the values for the dimensions shown in the illustration.

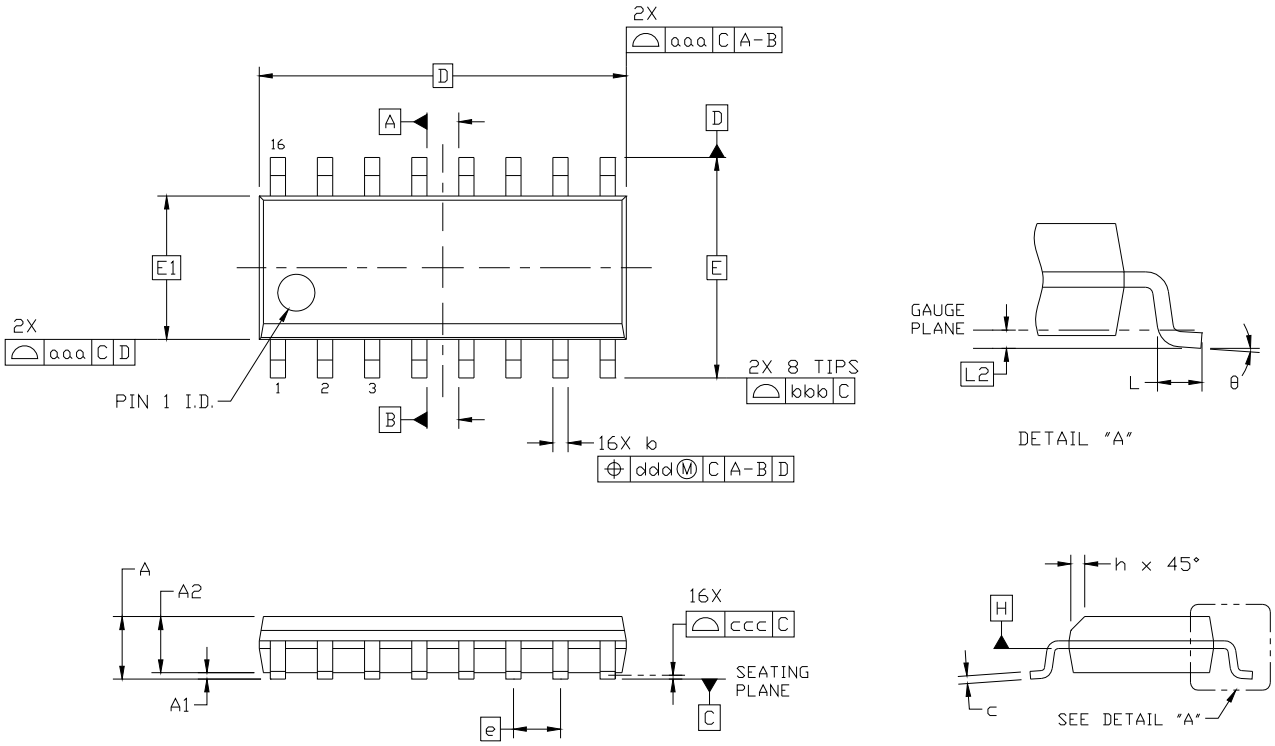


Figure 17. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 17. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Land Pattern: 16-Pin Narrow Body SOIC

Figure 18 illustrates the recommended land pattern details for the Si864x in a 16-pin narrow-body SOIC. Table 18 lists the values for the dimensions shown in the illustration.

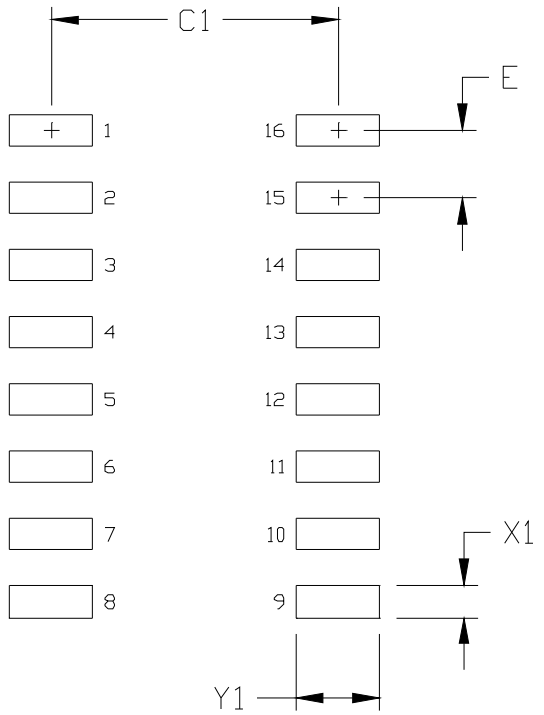


Figure 18. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 18. 16-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

10. Package Outline: 16-Pin QSOP

Figure 19 illustrates the package details for the Si864x in a 16-pin QSOP package. Table 19 lists the values for the dimensions shown in the illustration.

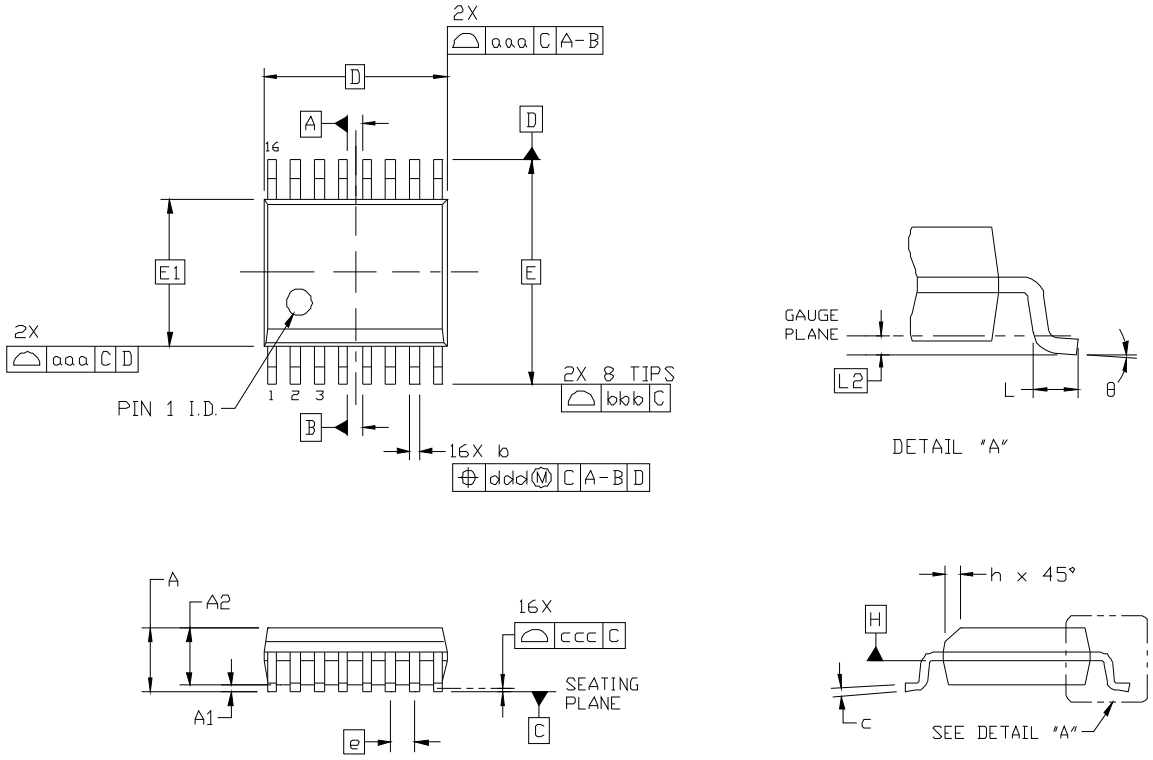


Figure 19. 16-pin QSOP Package

Table 19. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.20	0.30
c	0.17	0.25
D	4.89 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.635 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

11. Land Pattern: 16-Pin QSOP

Figure 20 illustrates the recommended land pattern details for the Si864x in a 16-pin narrow-body SOIC. Table 20 lists the values for the dimensions shown in the illustration.

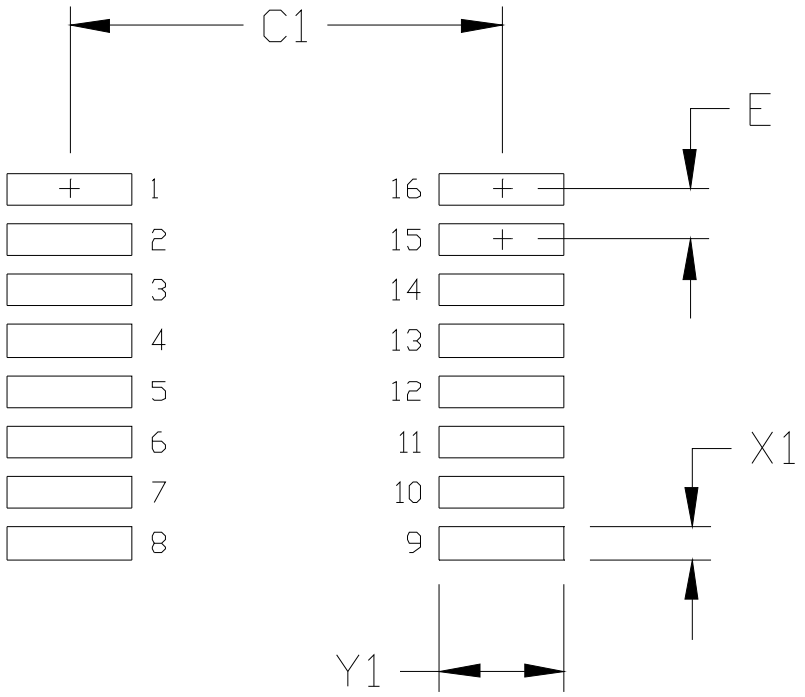


Figure 20. 16-Pin QSOP PCB Land Pattern

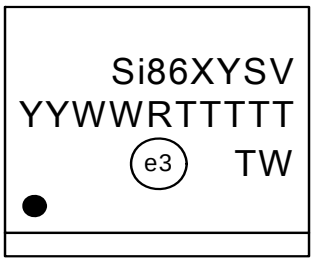
Table 20. 16-Pin QSOP Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	0.635
X1	Pad Width	0.40
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOP63P602X173-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05mm is assumed.

12. Top Markings

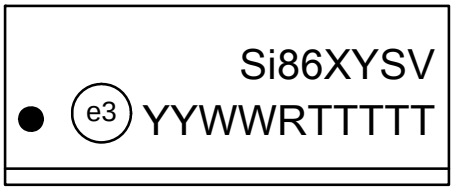
12.1. Top Marking (16-Pin Wide Body SOIC)



12.2. Top Marking Explanation (16-Pin Wide Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si86 = Isolator product series XY = Channel Configuration X = # of data channels (4, 3, 2, 1) Y = # of reverse channels (2, 1, 0)* S = Speed Grade (max data rate) and operating mode: A = 1 Mbps (default output = low) B = 150 Mbps (default output = low) D = 1 Mbps (default output = high) E = 150 Mbps (default output = high) V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date.
	RTTTTT = Mfg Code	Manufacturing code from assembly house “R” indicates revision
Line 3 Marking:	Circle = 1.5 mm Diameter (Center-Justified)	“e3” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan
***Note:** Si8645 has 0 reverse channels.		

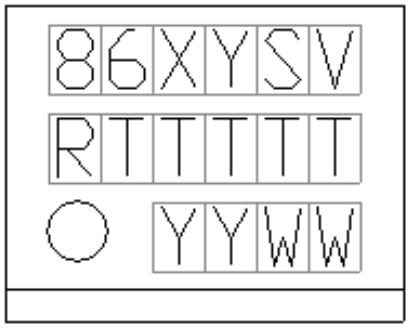
12.3. Top Marking (16-Pin Narrow Body SOIC)



12.4. Top Marking Explanation (16-Pin Narrow Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si86 = Isolator product series XY = Channel Configuration X = # of data channels (4, 3, 2, 1) Y = # of reverse channels (2, 1, 0)* S = Speed Grade (max data rate) and operating mode: A = 1 Mbps (default output = low) B = 150 Mbps (default output = low) D = 1 Mbps (default output = high) E = 150 Mbps (default output = high) V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV
Line 2 Marking:	Circle = 1.2 mm Diameter	“e3” Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	RTTTTT = Mfg Code	Manufacturing code from assembly house “R” indicates revision
***Note:** Si8645 has 0 reverse channels.		

12.5. Top Marking (16-Pin QSOP)



12.6. Top Marking Explanation (16-Pin QSOP)

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	86 = Isolator product series XY = Channel Configuration X = # of data channels (4, 3, 2, 1) Y = # of reverse channels (2, 1, 0)* S = Speed Grade (max data rate) and operating mode: A = 1 Mbps (default output = low) B = 150 Mbps (default output = low) D = 1 Mbps (default output = high) E = 150 Mbps (default output = high) V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV
Line 2 Marking:	RTTTTT = Mfg Code	Manufacturing code from assembly house “R” indicates revision
Line 3 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
***Note:** Si8645 has 0 reverse channels.		

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Added chip graphics on page 1.
- Moved Tables 1 and 11 to page 17.
- Updated Table 6, “Insulation and Safety-Related Specifications,” on page 14.
- Updated Table 8, “IEC 60747-5-2 Insulation Characteristics for Si86xxxx*,” on page 15.
- Moved Table 12 to page 20.
- Moved Table 13 to page 21.
- Moved “Typical Performance Characteristics” to page 24.
- Updated "4. Pin Descriptions" on page 25.
- Updated "5. Ordering Guide" on page 26.

Revision 0.2 to Revision 1.0

- Reordered spec tables to conform to new convention.
- Removed “pending” throughout document.

Revision 1.0 to Revision 1.1

- Updated High Level Output Voltage VOH to 3.1 V in Table 3, “Electrical Characteristics,” on page 8.
- Updated High Level Output Voltage VOH to 2.3 V in Table 4, “Electrical Characteristics,” on page 11.

Revision 1.1 to Revision 1.2

- Updated Table 14, “Ordering Guide for Valid OPNs[1,2],” on page 26.
  - Updated Note 1 with MSL2A.
  - Updated Current Revision Devices.

Revision 1.2 to Revision 1.3

- Updated "5. Ordering Guide" on page 26 to include MSL2A.

Revision 1.3 to Revision 1.4

- Updated Table 11 on page 17.
  - Added junction temperature spec.
- Updated "3.3.1. Supply Bypass" on page 23.
- Removed “3.3.2 Pin Connections” on page 23.
- Updated "4. Pin Descriptions" on page 25.
  - Updated table notes.
- Updated "5. Ordering Guide" on page 26.
  - Removed Rev A devices.
- Updated "6. Package Outline: 16-Pin Wide Body SOIC" on page 27.
- Updated Top Marks.
  - Added revision description.

Revision 1.4 to Revision 1.5

- Updated "5. Ordering Guide" on page 26.
- Updated "12.5. Top Marking (16-Pin QSOP)" on page 38.

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